19.8 A Polynomial-Predistortion Transmitter for WCDMA

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Predistortion techniques have been investigated in 3rd-generation cellular systems such as wideband code-division multiple access (WCDMA) in order to obtain both high linearity and high efficiency in handset power amplifiers (PAs) [1]. Analog baseband complex polynomial predistortion is appropriate for handsets because it can be completely integrated and does not require either a high-speed DAC or a complicated digital signal processing [1], [2]. The order of the polynomial predistortion, taking into account the power consumption, the size, and the noise, limits the applicable output power of the PA. However, it can be used up to the maximum output power of the PA by eliminating the fundamental component from the distortion components [3]. This paper describes an analog baseband complex polynomial predistortion transmitter IC, which can be used up to the maximum output power of the PA.

Figure 19.8.1 shows the block diagram of the predistortion transmitter IC that implements a 5th-order complex polynomial predistorter. When the predistorter is off, the adder passes the I/Q signals through to the I/Q Modulator. When the predistorter is on, the adder adds the 3rd- and the 5th-order distortion components to the original I/Q signals. The predistorter consists of 7-linear Gilbert cell mixers, 12 PGAs, and an HPF. Predistorted I/Q signals I_{out} and Q_{out} are given by

$$I_{out} + j \cdot Q_{out} = (I_{in} + j \cdot Q_{in}) \cdot \left\{ \begin{array}{l} 1 + A_3 \cdot e^{j \cdot B_3} \cdot \left(I_{in}^2 + Q_{in}^2 - DC_{env} \right) \\ + A_5 \cdot e^{j \cdot B_5} \cdot \left(I_{in}^2 + Q_{in}^2 - DC_{env} \right)^2 \end{array} \right\}$$

where I_{in} and Q_{in} are the original I/Q signals. A_3 and A_5 are respectively the 3rd- and the 5th-order magnitude coefficients, B_3 and B_5 are respectively the 3rd- and the 5th-order phase coefficients, DC_{env} is the average voltage of the envelope ($I_{in}^2 + Q_{in}^2$) and is subtracted from ($I_{in}^2 + Q_{in}^2$) by the HPF. The subtraction of DC_{env} is essential for the polynomial predistorter to operate effectively up to the maximum output power of the PA because the fundamental component $(I_{in} + j \cdot Q_{in}) \cdot DC_{env}$ generates an extra distortion product that weakens the effectiveness of the predistorter [3]. By adjusting these coefficients the 3rd- and 5th-order distortion products of the PA are cancelled out. To support many kinds of PA modules, the control ranges and steps of the coefficients are determined by measuring the characteristic of the PA modules beforehand. Four programmable coefficients, A_3, A_5, B_3, and B_5, are individually controlled by the PGAs. The PGAs of A_3 and A_5 provide 30dB control ranges with 1dB steps. The PGAs of B_3 and B_5 provide a 360° control range with 15° steps. Figure 19.8.2 shows the PGA of the phase shifter. The phase shifter sets the phase of the I/Q signals by multiplying sin(B) and cos(B) by the I/Q signals as the equation in Fig. 19.8.2. The PGA provides multiplication by the sine and the cosine of 360° in 15° steps by combining 7 different gains and both polarities. The phase-shifted I/Q signals are multiplied by ($I_{in}^2 + Q_{in}^2 - DC_{env}$), amplified by the PGAs for amplitude tuning and added to the original I/Q signals, as shown in Fig. 19.8.1. HPF consists of a 3pF on-chip capacitor and an MOS resistor and has a cutoff frequency of 10kHz. Since the nonlinear characteristics of the PA vary with output power, frequency, supply voltage and temperature, the handset has to provide the look-up tables and control the coefficients of the chip via 3-wire interface once at the slot time (0.66ms). The transmitter IC includes 3 RF paths and supports 4 frequency bands of 2GHz, 1.9GHz, 1.7GHz, and 800MHz. The I/Q Modulator has a direct-conversion architecture. The transmit signal is upconverted directly to RF by the quadrature LO signals derived from a double-frequency VCO for 2GHz, 1.9GHz, and 1.7GHz, and a four-times frequency VCO for 800MHz. The variable-gain range for each RF path is 85dB by analog control.

To test the effectiveness of the predistorter, a GaAs HBT PA module for 1.9GHz WCDMA handset is used. The original maximum output power of this PA is specified as 27dBm at $3.1V < V_{CC} < 3.4V$. Figure 19.8.3 shows the measured adjacent-channel leakage power ratio (ACLR) and current draw versus supply voltage of the PA at 1.95GHz with and without predistortion. In this figure, for all supply voltages, the output power of the PA is maintained at 27dBm using a WCDMA uplink signal. The difference in the current draw with and without predistortion of the PA is less than 1mA, and the predistorter improves ACLR. In other words, the predistorter reduces power consumption of the PA from 1333mW (3.3V×404mA) to 1091mW (2.7V×404mA) by 18% while maintaining a 5MHz offset ACLR of –43dBc. On the other hand, the power consumption of the predistorter is 17mW (2.4V×7mA) which is minimal.

Figure 19.8.4 shows the measured ACLR versus output power of the PA. The predistorter raises the output power of the PA by 1.5dB from 27.5dBm to 29dBm while maintaining the 5MHz offset ACLR of –43dBc. This means that in an optimized PA the size of the transistor will be reduced by 29%. Figure 19.8.5 shows measured output spectrum of the PA with and without predistortion under V_{CC}=3.4V and P_{out}=28dBm. Figure 19.8.6 summarizes the performance of the transmitter IC. The output noise density of the chip is –127dBm/Hz (12.5MHz offset) when the output power of the chip is 0dBm with the predistortion function. The chip satisfies the spurious emissions (1893.5MHz to 1919.6MHz) specification of 3GPP [4] that the in-band noise power shall be lower than –120dBc/Hz.

The IC is fabricated using a 0.18µm SiGe BiCMOS process. A die micrograph is shown in Fig. 19.8.7 and the total die area is 19.4mm^2 including an area reserved for future development. The sum of the areas of the 4 blocks surrounded by solid lines in Fig. 19.8.7 is 5.6mm^2. The transmitter draws 64mA and 57mA from a 2.4V supply with and without predistortion, respectively.

Acknowledgements:
The authors would like to acknowledge the MSD members in Sony, Atsugi, for their contribution in evaluation.

References:
[1] E. Westesson and L. Sundström, "Low-Power Complex Polynomial Predistorter Circuit in CMOS for RF Power Amplifier Linearization," *Proc. ESSCIRC*, pp. 486-489, Sept., 2001.
[2] T. Rahkonen, T. Kankaala, and M. Neitola, "A Programmable Analog Polynomial Predistortion Circuit For Linearising Radio Transmitters," *Proc. ESSCIRC*, pp. 276-279, Sept., 1998.
[3] N. Mizusawa and S. Kusunoki, "Third- and Fifth-Order Baseband Component Injection for Linearization of the Power Amplifier in a Cellular Phone," *IEEE Trans. Microwave Theory and Techniques,* vol. 53, pp. 3327-3334, Nov., 2005.
[4] TS 34.121 V 6.2.0, "Terminal Conformance Specification: Radio Transmission and Reception (FDD)," 3rd-Generation Partnership Project, Oct. 2005.

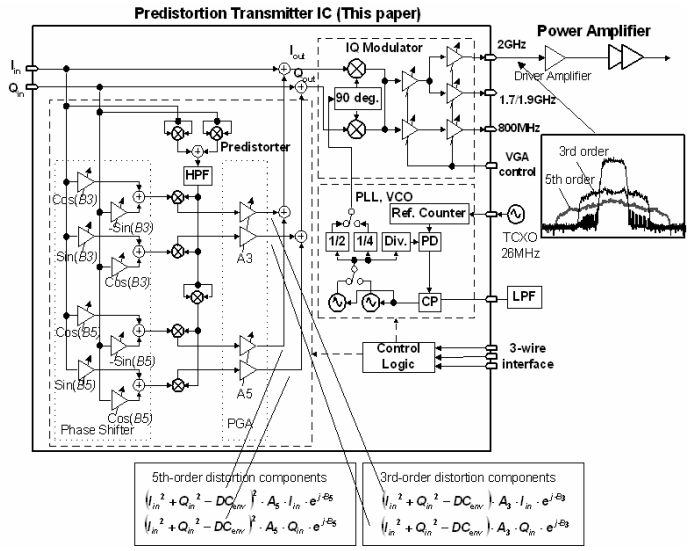

Figure 19.8.1: Block diagram of the predistortion transmitter.

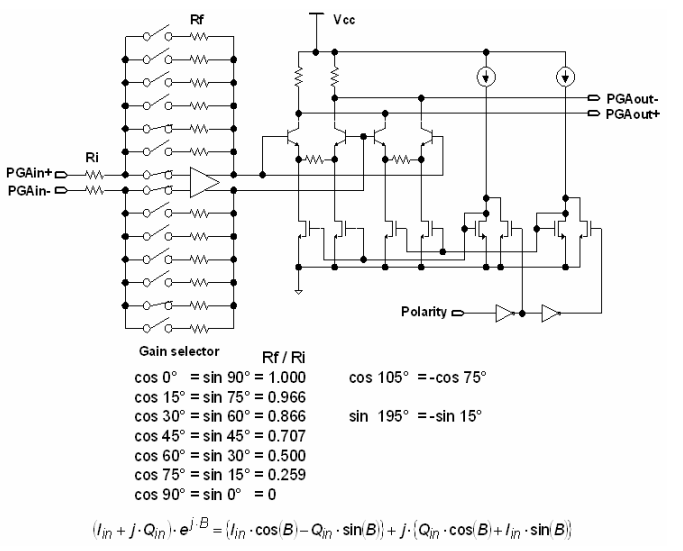

Figure 19.8.2: PGA of the phase shifter.

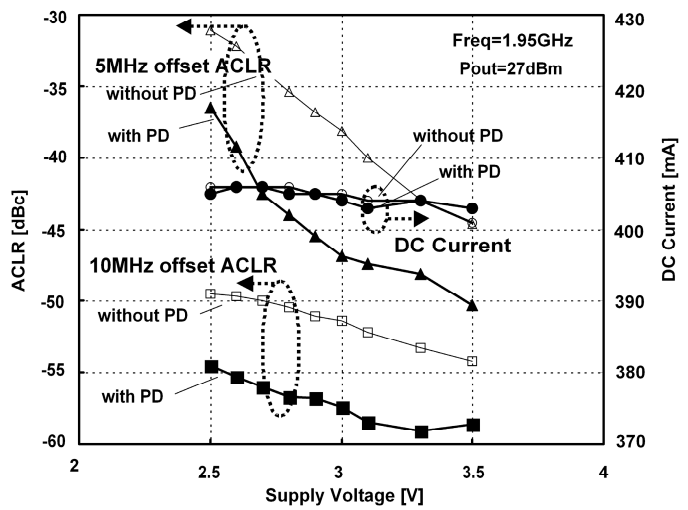

Figure 19.8.3: ACLR versus supply voltage of the PA.

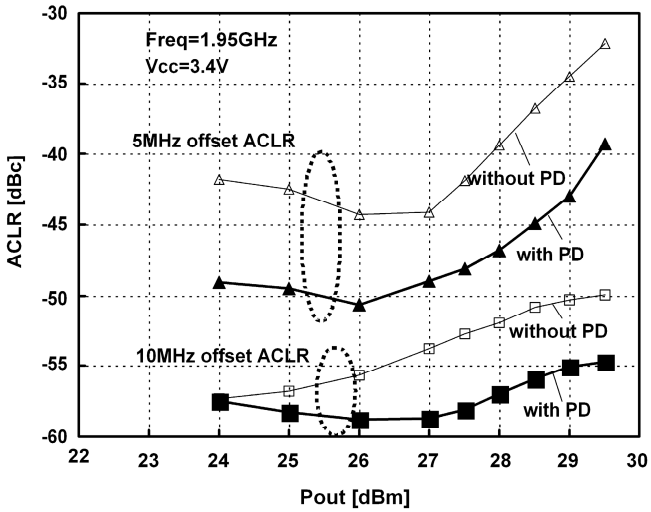

Figure 19.8.4: ACLR versus output power of the PA.

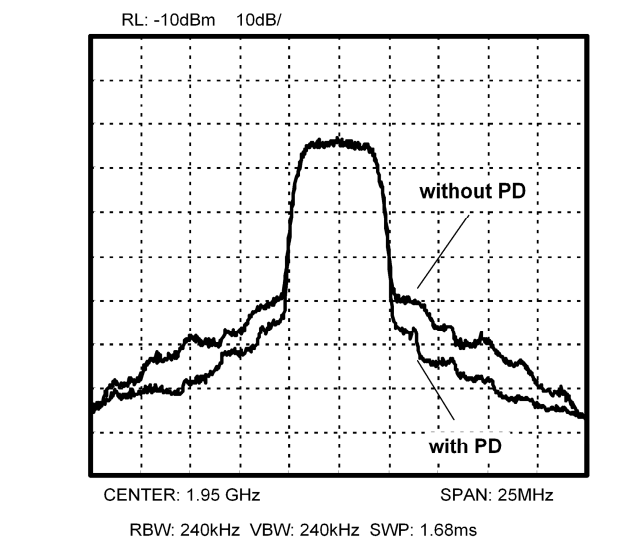

Figure 19.8.5: Measured spectrum of PA output.

Technology		0.18 um SiGe BiCMOS
Frequency bands		2GHz (1920 to 1980MHz) 1.9GHz (1850 to 1910MHz) 1.7GHz (1710 to 1785MHz) 0.8GHz (824 to 849MHz)
Maximum output power		0 dBm
EVM		5.5% rms
RF variable gain range		85 dB
Predistorter magnitude control range		30dB in 1dB steps
Predistorter Phase control range		360 degrees in 15-degree steps
In-band noise at maximum output power	12.5MHz offset	-127dBm/Hz
	40MHz offset	-131dBm/Hz
Current consumption (Vcc = 2.4V)	Predistortion OFF	57mA
	Predistortion ON	64mA

Figure 19.8.6: Summary of transmitter IC performance.

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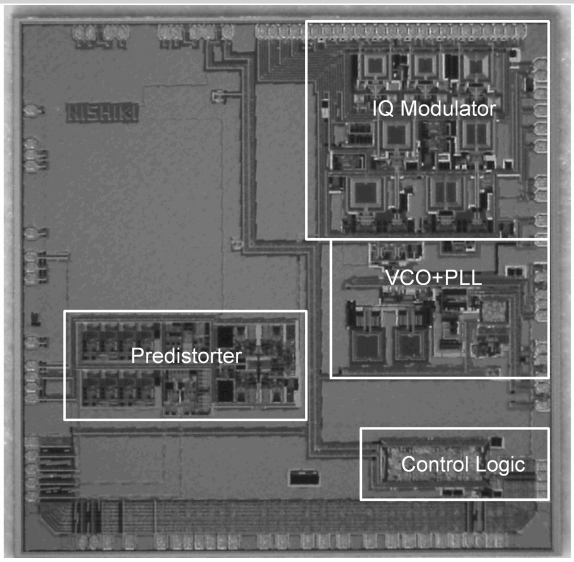

Figure 19.8.7: Chip micrograph.

